

BACKGROUND-CALIBRATING PIPELINED ANALOG-TO-DIGITAL CONVERTER

Abstract

A multiplying digital-to-analog converter (MDAC) stage includes a plurality of second capacitances in parallel selectively connected between an input node and an amplifier input and between a corresponding plurality of digital reference signals, which can include a pseudo-random first calibration signal, and the amplifier input. A pipelined ADC incorporating a series of such MDAC stages includes a multiplier connected to the last MDAC stage of the series, a low-pass filter for filtering output of the multiplier and outputting a DC component, and an encoder for receiving output of the MDAC stages and generating a digital output signal and for compensating the digital output signal with the DC component. Background calibration of the ADC includes applying the first calibration signal to a second capacitance of the MDAC stage during a hold phase, and filtering the first calibration signal from the digital output of the pipelined analog-to-digital converter.